#9/c
3/4/03 Mollis L

PATENT
81738.0292

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
KOJIMA, et al.
Serial No: 09/803,624
Filed: March 9, 2001
For: SMALL GEOMETRY HIGH VOLTAGE SEMICONDUCTOR DEVICE

Art Unit: 2815
Examiner: FENTY, J.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington D.C. 20231, on
February 11, 2003
Date of Deposit
Dariush G. Adli Reg. No. 51,386
Name
Signature 2/11/03
Date

AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated August 13, 2002, the period for response having been extended to February 13, 2003 by the accompanying Petition For Extension Of Time, please amend the above-identified application as follows. A marked-up copy, showing the changes made thereto, is appended.

IN THE CLAIMS:

Please amend Claim 28 and add new claims 30 to 35 as follows. A marked up copy of the amended claim, showing the changes made thereto, is attached. The claims, as pending in the present application, are as follows:

27. (Not Changed From Previous Version) A semiconductor integrated circuit according to claim 28, wherein the minimum gate length in the channel length direction of the LVMISFET is in the range of 1.5 – 2.5 μm.

C1

28. (Twice Amended) A semiconductor integrated circuit comprising: an HVMISFET (high withstand voltage MOSFET) having: